CLAIMS:

1. Switched mode power supply assembly (1) comprising at least two switched mode power supply units (10_i) coupled to each other in parallel;

each power supply unit (10_i) having an output stage (50_i, 60_i) capable of selectively operating in a first mode wherein its output signal ($I_{OUT,i}$) is increasing and operating in a second mode wherein its output signal ($I_{OUT,i}$) is decreasing;

a control device (100) receiving mode switch control signals from all power supply units (10_i);

wherein the control device (100), if it finds that the actual phase relationship between two power supply units deviates from an optimal phase relationship, is designed to generate synchronising control signals for at least one power supply unit (10_2), effectively changing the timing of at least one mode switch moment, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced.

2. Switched mode power supply assembly (1) comprising a plurality of at least two switched mode power supply units (10_i) coupled to each other in parallel;

each power supply unit (10_i) having an output stage (50_i, 60_i) for generating an output signal ($I_{OUT,i}$), the output stage (50_i, 60_i) being capable of selectively operating in a first mode wherein the output signal ($I_{OUT,i}$) is increasing and operating in a second mode wherein the output signal ($I_{OUT,i}$) is decreasing;

each power supply unit (10_i) having mode switch control means (30_i) for generating a first mode switch control signal (Ri) controlling the output stage (50_i, 60_i) to switch from its first operating mode to its second operating mode, and for generating a second mode switch control signal (Si) controlling the output stage (50_i, 60_i) to switch from its second operating mode to its first operating mode;

the switched mode power supply assembly (1) further comprising a control device (100) having inputs (121, 122, 123, 124) receiving the mode switch control signals from all power supply units (10_i);

wherein the control device (100) is designed to determine an optimal phase relationship between the phases of the mode switch control signals of one power supply unit

(10_2) and the phases of the mode switch control signals of at least one reference power supply unit (10_1);

wherein the control device (100) is designed to compare the phases of the mode switch control signals of said one power supply unit (10_2) with the phases of the mode switch control signals of said at least one reference power supply unit (10_1);

and wherein the control device (100), if it finds that the actual phase relationship deviates from said optimal phase relationship, is designed to generate synchronising control signals for said one power supply unit (10_2) and/or said at least one reference power supply unit (10_1), effectively changing the timing of at least one mode switch moment of said one power supply unit (10_2) and/or of said at least one reference power supply unit (10_1), respectively, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced, in order to ensure interleaved operation of all units.

3. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100), if it finds that said one power supply unit (10_2) is lagging with respect to said optimal phase relationship, is designed to generate a delaying synchronising control signal ($SCDH_1$, $SCDL_1$) for said at least one reference power supply unit (10_1), effectively delaying the timing of at least one mode switch moment of said at least one reference power supply unit (10_1).

4. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100), if it finds that said one power supply unit (10_2) is lagging with respect to said optimal phase relationship, is designed to generate an advancing synchronising control signal ($SCAH_2$, $SCAL_2$) for said one power supply unit (10_2), effectively advancing the timing of at least one mode switch moment of said one power supply unit (10_2).

5. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100), if it finds that said one power supply unit (10_2) is early with respect to said optimal phase relationship, is designed to generate a delaying synchronising control signal ($SCDH_2$, $SCDL_2$) for said one power supply unit (10_2), effectively delaying the timing of at least one mode switch moment of said one power supply unit (10_2).

6. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100), if it finds that said one power supply unit (10_2) is early with respect to said optimal phase relationship, is designed to generate an advancing synchronising control signal ($SCAH_1$, $SCAL_1$) for said at least one reference power supply unit (10_1), effectively advancing the timing of at least one mode switch moment of said at least one reference power supply unit (10_1).

7. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100) is designed to generate its synchronising control signals such that the phase mismatch is completely compensated in one step.

8. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100) is designed to generate its synchronising control signals such that the phase mismatch is reduced by a predetermined constant factor K2.

9. Switched mode power supply assembly (1) according to claim 2, wherein the control device (100) is designed to calculate a first time difference (|t21-t13|) between a first time (t21) when the output signal (SM2) of said one power supply unit (10_2) reaches a first boundary level (S_{BH}) and a second time (t13) when the output signal (SM1) of said at least one reference power supply unit (10_1) reaches the same first boundary level (S_{BH});

wherein the control device (100) is designed to calculate a second time difference (|t23-t13|) between said second time (t13) and a third time (t23) when the output signal (SM2) of said one power supply unit (10_2) reaches said first boundary level (S_{BH}) again;

wherein the control device (100) is designed to calculate the difference between said first time difference (|t21-t13|) and said second time difference (|t23-t13|);

wherein the control device (100) is designed to divide said calculated difference by a predetermined factor (K2) to yield a delay time (|t31-t23|);

and wherein the control device (100) is designed to generate a delaying synchronising control signal ($SCDH_2$) for said one power supply unit (10_2) such that said one power supply unit (10_2) switches its operating mode at a delayed switching time (t31) calculated as the said third time (t23) plus said delay time (|t31-t23|).

10. Switched mode power supply assembly (1) according to claim 2, wherein the output stage (50_i, 60_i) comprises at least one input (R; S) coupled to an output of an AND gate (141, 142), this AND gate (141, 142) having an input receiving a command signal (R1; S1) from the corresponding mode switch control means (30_i) and having another input receiving a delaying synchronising control signal (SCDH1, SCDL1) from the control device (100).

11. Switched mode power supply assembly (1) according to claim 2, wherein the output stage (50_i, 60_i) comprises at least one input (R; S) coupled to an output of an OR gate (161, 162), this OR gate (161, 162) having an input receiving a command signal (R1; S1) from the corresponding mode switch control means (30_i) and having another input receiving an advancing synchronising control signal (SCAH1, SCAL1) from the control device (100).

12. Switched mode power supply assembly (1) according to claim 2, wherein all power supply units (10) are mutually identical.

13. Switched mode power supply assembly (1) according to claim 2, wherein each power supply unit (10_i) comprises a target signal input (16_i), all target signal inputs of all power supply units being connected in parallel to one common target signal source (S_{TARGET}).

14. Switched mode power supply assembly (1) according to claim 2, wherein each power supply unit (10_i) comprises a current output (13_i), all current outputs of all power supply units being connected in parallel to one common assembly output (3).

15. Switched mode power supply assembly (1) according to claim 2, wherein each power supply unit (10_i) comprises a first supply input (11_i) and a second supply input (12_i), all first supply inputs of all power supply units being connected in parallel to one common high voltage supply source (V_{HIGH}), and all second supply inputs of all power supply units being connected in parallel to one common low voltage supply source (V_{LOW}).

16. Switched mode power supply assembly (1) according to claim 2, wherein said signal generating means comprise:

two controllable switches (61, 62) coupled in series between a first supply input (11) and a second supply input (12), a node (A) between said switches being coupled to said module output (13);

a switch driver (50) having outputs (52, 53) coupled to control inputs of respective switches (61, 62), the switch driver (50) being capable of operating in a first operative state in which it generates its control output signals such that the second switch (62) is non-conductive while the first switch (61) is in its conductive state, and being capable of operating in a second operative state in which it generates its control output signals such that the first switch (61) is non-conductive while the second switch (62) is in its conductive state;

a window comparator (30) having a high boundary input (32) and a low boundary input (33), a control output (34) coupled to a control input (51) of said switch driver (50), and a measuring signal input (36) coupled to receive said measuring signal (S_M) from said current sensor (67);

wherein the window comparator (30) is adapted to generate a first control signal commanding said switch driver (50) to enter its first operative state when said falling measuring signal (S_M) becomes equal to the signal level (S_{BL}) at its low boundary input (33), and to generate a second control signal commanding said switch driver (50) to enter its second operative state when said rising measuring signal (S_M) becomes equal to the signal level (S_{BH}) at its high boundary input (32).

17. Switched mode power supply assembly (1) according to claim 2, wherein the mode switch control means (30_i) are designed for generating a first mode switch control signal (Ri) controlling the output stage (50_i, 60_i) to switch from its first operating mode to its second operating mode if the rising output signal ($I_{OUT,i}$) reaches a first boundary level (S_{BH}) and for generating a second mode switch control signal (Si) controlling the output stage (50_i, 60_i) to switch from its second operating mode to its first operating mode if the falling output signal ($I_{OUT,i}$) reaches a second boundary level (S_{BL}).

18. Switched mode power supply assembly (1) according to any of the previous claims, wherein the power supply modules are implemented as DC/DC converter modules.

19. Switched mode power supply assembly (1) according to any of the previous claims, wherein the power supply modules are implemented as DC/AC inverter modules.

20. Solar cell assembly, comprising a boost converter for up-converting the output voltage of the solar cells, having its output voltage coupled to a DC/AC inverter, wherein either said boost converter or said inverter, or both, comprise a switched mode power supply assembly (1) according to any of the previous claims.

21. Driver for driving a lamp such as a gas discharge lamp, comprising a switched mode power supply assembly (1) according to any of the previous claims as a DC/AC inverter for generating supply current for the lamp.

22. Actuator for a motion control apparatus, comprising a switched mode power supply assembly (1) according to any of the previous claims.